40G QSFP+ Active Optical Cable

ESAOC003

Product Features

- Support Data Rate 41.25Gbps
- Compliant with SFF-8436 rev.4.8, IEEE 802.3ba
- GR-468-core
- Full duplex 4 channel 850nm parallel AOC
- Multirate capability: 1.06Gb/s to 10.5Gb/s per channel
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- DDM function implemented
- Single MPO connector receptacle
- Hot Pluggable QSFP+ form factor
- Single +3.3V power supply
- Power consumption less than 1W
- Operating range 0~+70°C case temperature
- Standard lengths of 3, 5, 10, 15, 20, 30, 50 and 100m

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	T_S	-40	+85	°C
Supply voltage	V_{CC3}	0	3.6	V
Relative humidity	RH	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	TC	0		70	°C
Power Dissipation	PD			1	W

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Parameter	Symbol	Min.	Typ.	Max.	Unit
Data Rate			41.25		Gbps
Standard Cable Lengths		3, 5, 10, 15, 20, 30, 50 & 100m			m

Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	Vcc1 VccTx VccRx		3.15		3.45	v
Supply Current	Icc				300	mA
Differential data input swing (note 1)	Vin,pp		180		1200	mVpp
Differential input threshold				50		mV
Differential data output swing (note 2, 3)	Vout,pp		0		800	mVpp
Power Supply Ripple Tolerance	PSR		50			mVpp
Reference Differential Input Impedance	Zd			100		Ω
Termination Mismatch (note 4)	ΔZM				5	%
Input AC Common Mode Voltage					25	mV (RMS)
Differential Input Return Loss (note 5, 6)	SDD11	0.01-4.1 GHz				dB
		4.1 – 11.1 GHz				dB
Differential to Common Mode Loss	SCD11	0.01-11.1 GHz			-10	dB
Jitter Tolerance (Total)	TJ				0.40	UI
Jitter Tolerance (Deterministic)	DJ				0.15	UI
Reference Differential Output Impedance	Zd			100		Ω
Termination Mismatch	ΔZM				5	%
Output AC Common Mode Voltage					15	mV_{RMS}
Output Rise and Fall time (20% to 80%)	tRH, tFH		24			ps
Differential Output Return Loss (note 7,8)	SDD22	0.01-4.1 GHz				dB
		4.1 – 11.1 GHz				dB
Common Mode Output Return Loss (note 9)	SCC22	0.01-2.5 GHz				dB
		2.5-11.1 GHz			-3	dB
Deterministic Jitter (note 10)	DJOUT				0.38	UI
Total Jitter (note 10)	TJOUT				0.64	UI

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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low Frequency 3dB Cutoff	fc		175			
Max Bit Rate NRZ	B				12.5	
Ch / Ch crosstalk					-26	dB
Output Pre-emphasis settings (user selectable)	PE			0		mV
				125		mV
				175		mV
				325		mV
Pre-Emphasis pulse width			60		90	ps
Channel Latency				TBD		
Channels Skew				TBD		
Digital clock to data delay					25	ns
Digital output rise/fall times					5	ns
Digital input / output Cap					1	pF
Digital input logic High			2			V
Digital input logic Low					1	V
ESD Signal pads					500	V
ESD (other pads)					2	kV

Notes:

1. AC coupled internally. See Figure 2 for input eye mask requirements. Self-biasing 100Ω differential input.
2. AC coupled with 100Ω differential output impedance. See Figure 3 for output eye mask.
3. Settable in 4 discrete steps.
4. See SFF-8431 Rev 3.2 (SFP+) section D.15 Termination Mismatch for definition & test recommendations.
5. Reflection coefficient given by equation SDD11(dB)< -12+2*SQRT(f), with f in GHz.
6. Reflection coefficient given by equation SDD11(dB)< -6.3+13Log10(f/5.5), with f in GHz.
7. Reflection coefficient given by equation SDD22(dB)< -12+2*SQRT(f), with f in GHz.
8. Reflection coefficient given by equation SDD22(dB)< -6.3+13Log10(f/5.5), with f in GHz.
9. Reflection coefficient given by equation SCC22(dB)< -7+1.6*f, with f in GHz.
10. When transmitter input jitter specs are met.

Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Initialization time	t_init			2000	ms	
Reset Init Assert Time	t_reset_init			2	us	
Serial Bus Hardware Ready Time	t_serial			2000	ms	
Reset Assert Time	t_reset			2000	ms	

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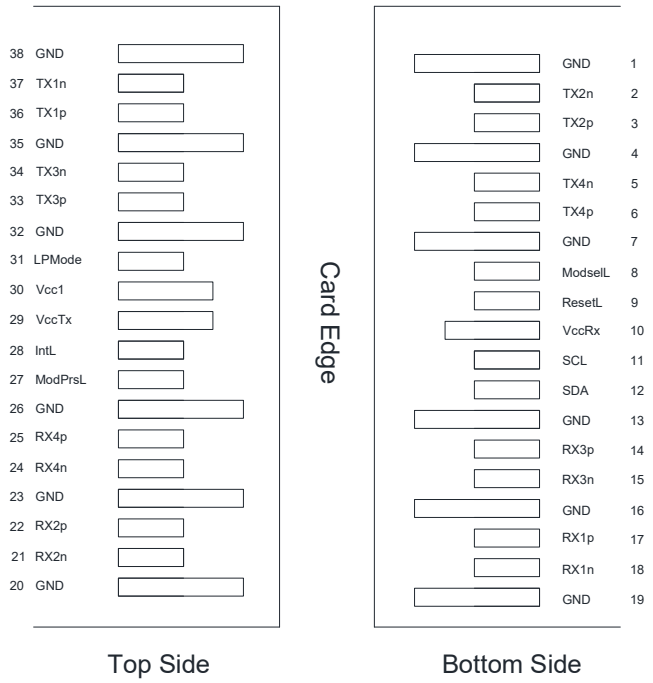
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LPMode Assert Time	ton_LPMode			100	us	
LPMode Deassert Time	Toff_LPMode			300	ms	
IntL Assert Time	ton_IntL			200	ms	
IntL Deassert Time	toff_IntL			500	us	
Rx LOS Assert Time	ton_los			100	ms	
Tx Fault Assert Time	ton_Txfault			200	ms	
Flag Assert Time	ton_flag			200	ms	
Mask Assert Time	ton_mask			100	ms	
Mask Deassert Time	toff_mask			100	ms	
Power_overrideor Power_set Assert Time	ton_Pdown			100	ms	
Power_override or Power_set Deassert Time	toff_Pdown			300	ms	
Two wire Serial Interface Clock Rate			100	400	KHz	
Power Supply Noise				50	mVpp	

Pin Descriptions



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Pin	Symbol	Descriptions	Note
1	GND	Ground	1
2	Tx2n	Transmitter inverted data input	
3	Tx2p	Transmitter non-inverted data input	
4	GND	Ground	1
5	Tx4n	Transmitter inverted data input	
6	Tx4p	Transmitter non-inverted data input	
7	GND	Ground	
8	ModSelL	Module select	
9	ResetL	Module reset	
10	VccRx	+3.3V power supply receiver	2
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver non-inverted data output	
15	Rx3n	Receiver inverted data output	
16	GND	Ground	1
17	Rx1p	Receiver non-inverted data output	
18	Rx1n	Receiver inverted data output	1
19	GND	Ground	1
20	GND	Ground	
21	Rx2n	Receiver inverted data output	
22	Rx2p	Receiver non-inverted data output	
23	GND	Ground	
24	Rx4n	Receiver inverted data output	
25	Rx4p	Receiver non-inverted data output	
26	GND	Ground	1
27	ModPrsL	Module present	
28	IntL	Interrupt	
29	VccTx	+3.3V power supply transmitter	2
30	Vcc1	+3.3V power supply	2
31	LPMode	Low power mode	

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Pin	Symbol	Descriptions	Note
32	GND	Ground	1
33	Tx3p	Transmitter non-inverted data input	
34	Tx3n	Transmitter inverted data input	
35	GND	Ground	1
36	Tx1p	Transmitter non-inverted data input	
37	Tx1n	Transmitter inverted data input	
38	GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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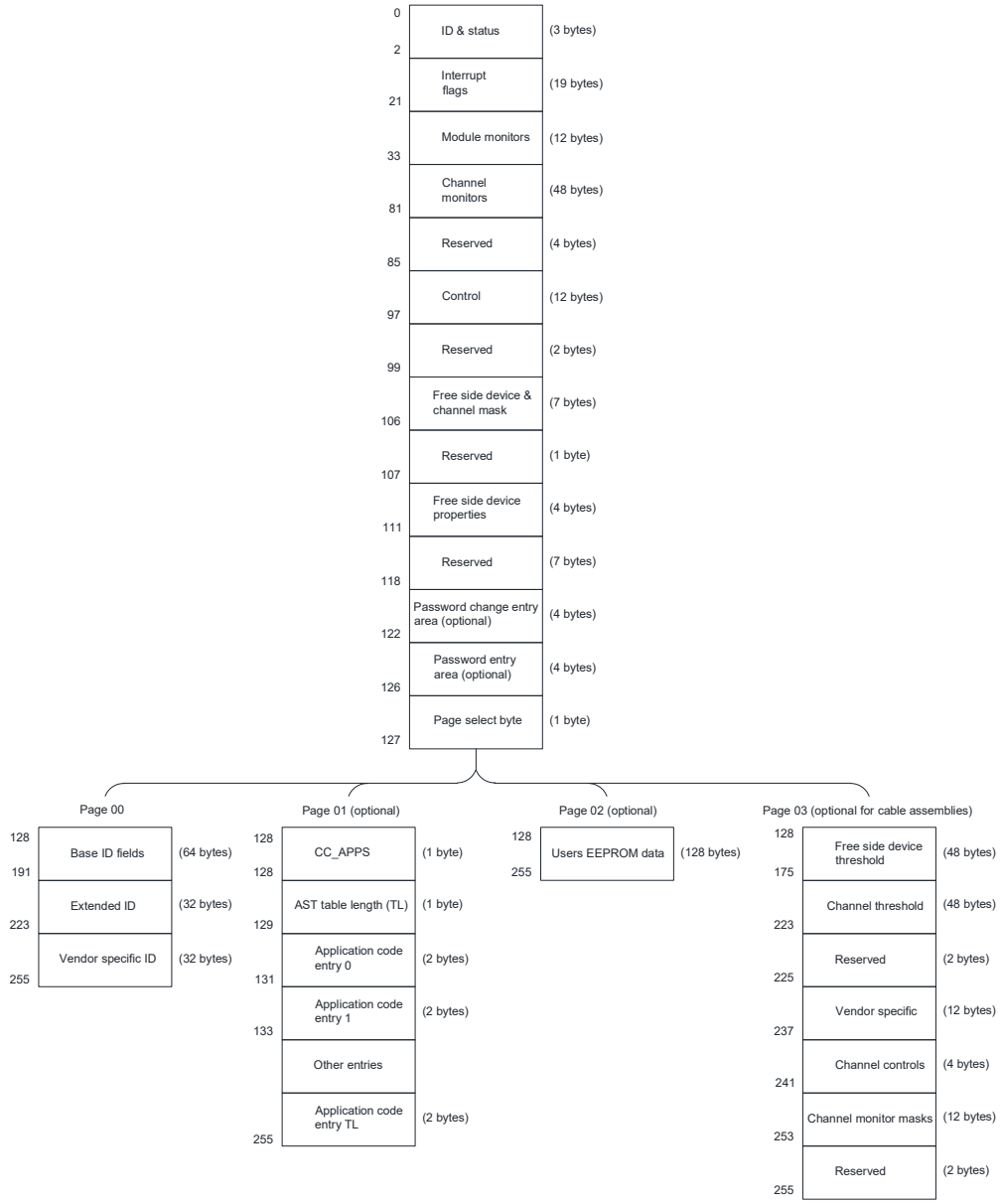
Digital Diagnostic Memory Map



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